

## CLAIMS

What is claimed is:

1. An on-chip capacitor, comprising:  
first and second metal patterns each in first and second levels;  
wherein said first pattern of said first level is connected to said first  
pattern of said second level by conducting vias;  
5 wherein said second pattern of said first level is connected to said  
second pattern of said second level by conducting vias; and  
wherein said first pattern and said second pattern form contacts for  
a capacitor.
2. The capacitor of Claim 1, wherein said first and second levels are  
separated by a material of first dielectric constant, and said first  
and second patterns are separated by a material of a second  
dielectric constant, and wherein said first dielectric constant is  
greater than said second dielectric constant.
3. The capacitor of Claim 1, wherein said vias extend over greater  
than half the length of said first and said second metal patterns  
where said patterns face each other.
4. The capacitor of Claim 1, wherein vias extend from said first and  
said second metal patterns and do not connect to metal patterns  
of any other level.

5. An integrated circuit structure, comprising:
- a first layer having a first metallization pattern comprising at least two metal lines;
  - a second layer having a second metallization pattern comprising at least two metal lines;
- 5 wherein said first and second metallization patterns are connected by conducting vias to form a capacitance.
6. The integrated circuit of Claim 5, wherein said first and said second metallization patterns are separated by a material of a first dielectric constant, and said vias are separated by a material of a second dielectric constant, said second dielectric constant being greater than said first dielectric constant.
7. The integrated circuit of Claim 5, wherein said vias extend at least half the length of said first and said second metallization patterns where they face each other.
8. The integrated circuit of Claim 5, further comprising vias extending from said first and second metallization patterns of said first layer that do not connect to any other metallization patterns.

9. An on-chip capacitor, comprising:  
a first stack of metal lines;  
a second stack of metal lines laterally separated from said first stack  
by a first dielectric material;  
5 wherein two or more of said metal lines of said first stack are  
vertically connected by conducting vias;  
wherein two or more of said metal lines of said second stack are  
vertically connected by conducting vias; and  
wherein said first stack and said second stack provide two terminals  
10 of a capacitor.
10. The method of Claim 9, wherein said vias are laterally separated  
by a second dielectric material, and said dielectric constant of  
said second dielectric material is greater than the dielectric  
constant of said first dielectric material.
11. The method of Claim 9, wherein said vias extend over half the  
length of said metal lines to which they connect.
12. An on-chip capacitor, comprising:  
first and second interdigitated metal patterns providing lateral  
capacitance therebetween;  
elongated vias which provide lateral capacitance therebetween, and  
5 which are parallel and electrically connected to each of said  
first and second patterns;  
wherein said first and second metal patterns, in combination with  
said elongated vias, define a capacitor.

13. The method of Claim 12, wherein said elongated vias extend over more than half the peripheral length where said first and said second interdigitated metal patterns face each other.
14. The method of Claim 12, wherein said elongated vias also provide vertical connection from said respective metal patterns to corresponding metal patterns in one or more other layers of metallization.
15. The method of Claim 12, wherein said elongated vias provide more lateral capacitance than said interdigitated metal patterns do.
16. The method of Claim 12, further comprising vias attached to said first and second patterns that do not connect to any other metal patterns.